REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-20 are pending in the present application. Claims 1, 12, 14, and 20 are amended by the present amendment.

In the outstanding Office Action, Claims 12-19 were rejected under 35 U.S.C. § 112, second paragraph, and Claims 1-20 were rejected under 35 U.S.C. § 103(a) as unpatentable over Iguchi et al. (U.S. Patent No. 6,693,049, herein "Iguchi").

Because the present amendment places the claims in better form for consideration on appeal by amending Claims 1, 14, and 20 to more clearly recite novel features of the present invention, entry of this amendment under 37 CFR § 1.116 is believed to be in order and it is therefore respectfully requested.

Regarding the rejection of Claims 12-19 under 35 U.S.C. § 112, second paragraph, Claim 12 has been amended to more clearly recite a relation among (i) a dummy wiring layer, (ii) a dummy via, and (iii) a dummy wiring pattern, and Claim 14 has been amended to recite that a wide width lower wiring layer has "a width wider than that of the narrow width lower wiring layer." The claim amendments find support in Figures 1 and 2 and their corresponding description in the specification. No new matter has been added. Accordingly, it is respectfully requested this rejection be withdrawn.

Regarding the rejection of Claims 1-20 under 35 U.S.C. § 103(a) as unpatentable over Iguchi, independent Claims 1, 14, and 20 have been amended to recite that "voids are generated at the second damaged region in the lower wiring layer of Cu or a Cu alloy to cause a contact defect between the dummy via and the lower wiring layer." The claim amendments find support in the specification, for example at page 10, lines 3-8, and in Figures 9A, 9B,

and 10 and their corresponding description in the specification. No new matter has been added.

Briefly recapitulating, amended independent Claim 1 is directed to a semiconductor device that includes a multi-layered wiring structure formed on a semiconductor substrate. Each of the wiring layers includes a metal wiring made of one of Cu and a Cu alloy. The multi-layered wiring structure includes, a lower wiring layer, a via connected between an upper wiring layer and a first damaged region formed on the lower wiring layer, and a dummy via that is not connected to the upper wiring layer but is connected to a second damaged region formed on the lower wiring layer. Voids are generated at the second damaged region in the lower wiring layer of Cu or Cu alloy to cause a contact defect between the dummy via and the lower wiring layer. Independent Claims 14 and 20 have been amended similar to Claim 1.

In a non-limiting example, Figure 1 shows the lower wiring layer 11, the upper wiring layer 12a-12c, the via 14, and the dummy via 16 that is not connected to the upper wiring layer 12a-12c.

Turning to the applied art, Iguchi shows in Figures 2(a)-(g) a semiconductor device having a substrate and a wiring layer made of Cu formed on the substrate. The outstanding Office Action states in the paragraph bridging pages 3 and 4 that Iguchi has "a lower wiring layer provided by the substrate itself." However, Applicant respectfully submits that the substrate of Iguchi is different than a wiring layer of Cu or Cu alloy.

In addition, Iguchi describes a method for filling a fine hole that is less than or equal to 0.18 μm.[1] Figures 2(a)-(g) of Iguchi show the Cu wiring formed within an interlayer on the substrate. Regarding the substrate, Iguchi discloses at column 2, lines 57-63, that "when the trench holes are formed through an etching process ..., if the surface of the substrate is

[1] Iguchi, column 1, lines 5-9.

exposed in the bottom of the via-hole, the surface of the substrate is damaged by the etching gas." Thus, Iguchi does not teach or suggest a lower wiring layer in which a second damaged region is formed as required by Claims 1, 14, and 20.

Further, Applicant respectfully submits that the nature of the damage that occurs when the surface of the substrate in Iguchi is exposed to the etching process is different from the damage that occurs when the surface of the Cu wiring of the device of Claim 1 is exposed to the etching process. As shown in Figures 9A, 9B and 10 of the specification, voids are generated at the etching-damaged surface of the Cu wiring to cause a contact defect at the dummy via contact. Thus, Applicant respectfully submits that the etching-caused damage that occurs at the Cu wiring according to the claimed invention is different from the defect that occurs at the Si substrate taught by Iguchi.

Accordingly, it is respectfully submitted that independent Claims 1, 14, and 20 and each of the claims depending therefrom patentably distinguish over Iguchi.

Consequently, in light of the above-discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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